Vishal Canumalla

github.com/vcanumalla vcanumalla.github.io

EDUCATION

Stanford University 09/2024 - Present

PHD ELECTRICAL ENGINEERING

- · Research Interests: Computer Architecture, Compilers, Formal Methods, Systems
- Rotation Advisor: Prof. Thierry Tambe

University of Washington

B.S. COMPUTER SCIENCE

09/2020 - 06/2024 GPA: 3.9 / 4.0

Advisor: Prof. Zachary Tatlock

Conference and Journal Publications

FPGA Technology Mapping Using Sketch-Guided Program Synthesis

ASPLOS 2024

Gus Henry Smith, Ben Kushigian, **Vishal Canumalla**, Andrew Cheung, Steven Lyubomirsky, Sorawee Porncharoenwase, René Just, Gilbert Louis Bernstein, Zachary Tatlock.

Application-Level Validation of Accelerator Designs Using a Formal Software/Hardware Interface TODAES 2023 Bo-Yuan Huang, Steven Lyubomirsky, Yi Li, Mike He, Thierry Tambe, Gus Henry Smith, Akash Gaonkar, **Vishal Canumalla**, Andrew Cheung, Gu-Yeon Wei, Aarti Gupta, Zachary Tatlock, Sharad Malik.

Workshop and Short Papers

There and Back Again: A Netlist's Tale with Much Egraphin'

LATTE 2024

Gus Henry Smith, Zachary D. Sisco, Thanawat Techaumnuawit, Jingtao Xia, **Vishal Canumalla**, Andrew Cheung, Zachary Tatlock, Chandrakana Nandi, Jonathan Balkind.

Generate Compilers from Hardware Models!

PLARCH 2023

Gus Henry Smith, Ben Kushigian, Vishal Canumalla, Andrew Cheung, René Just, Zachary Tatlock.

EXPERIENCE

Adobe Research 06/2024 - 09/2024

RESEARCH SCIENTIST INTERN

- · Prototyped a performance analysis compiler pass for Halide pipelines.
- · Advised by Dr. Derek Gerstmann.

UW Programming Languages & Software Engineering Group

05/2023 - 06/2024

RESEARCH ASSISTANT

- · Researched applications of program synthesis in hardware compilers for FPGAs.
- · Developing tools for porting and compiling hardware designs to diverse backends.

UW Systems, Machine Learning, and Architecture Lab

05/2021 - 05/2023

RESEARCH ASSISTANT

 Researched efficient compilation techniques to specialized accelerators, including hardware/software interfaces, verified operator mapping, and compiler optimizations.

Certora 03/2022 - 06/2022

RESEARCH INTERN

- · Prototyped mutation testing techniques for smart contract verification.
- · Advised by Dr. Chandrakana Nandi.

Posters and Presentations

October 2023. FPGA Technology Mapping Using Sketch-Guided Program Synthesis. *Allen School Annual Affiliate Research Showcase*, Seattle WA.

September 2023. Application of Sketch Guided Synthesis to Runtime Reconfigurable FPGA Primitives. *ICFP Student Research Competition*, Seattle WA.

May 2023. FPGA Synthesis via Program Synthesis. Allen School Undergraduate Research Showcase, Seattle WA.

November 2022. Specialized Accelerators: Addressing the Mapping Gap. *Allen School Annual Affiliate Research Showcase*, Seattle WA.

Honors, Awards, and Fellowships

- · NSF Graduate Research Fellowship (Honorable Mention) (2024)
- · ICFP Student Research Competition 3rd Place Winner (2023)

INVITED TALKS

April 2023. Replacing Accelerator APIs with a Formal Software/Hardware Interface. *UW PLSE Lunch Seminar* SKILLS

Languages: C++, Racket, Java, Rust, OCaml, Coq **Technologies:** TVM, Rosette, Spring, Git, CircleCl